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09/628,473	07/31/2000	Donald M. Gray	14531.73	5542

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EXAMINER	
PARK, ILWOO	

ART UNIT	PAPER NUMBER
2182	4

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/628,473	Applicant(s) GRAY ET AL.	
	Examiner Ilwoo Park	Art Unit 2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18-26* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-44 are presented for examination.

Claim Objections

2. Claim 37 is objected to because of the following informalities: the phraseology "DMA module" is inconsistent with the phraseology "DMA engine". Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-12, 15-17, 37-39 and 41-44 are rejected under 35 U.S.C. 102(e) as being anticipated by Parvin et al., US patent No. 6,167,465.

As to claims 1 and 7, Parvin et al teach a system having a data reservoir [FIFOs 306] storing channel data for one or more channels associated with one or more devices [col. 15, lines 16-22], a method for arbitrating data requests of the one or more channels to a main memory [RAM 212], the method comprising the acts of:

defining a circular list [col. 17, lines 44-50; fig. 15a] having a plurality of entries, wherein the entries correspond to the one or more channels;

evaluating [col. 12, lines 16-40] a channel associated with an entry in the circular list to determine whether the channel requires service; and

servicing [col. 15, lines 33-42] the channel by requesting channel data from the main memory to replenish [col. 12, lines 33-36] the data reservoir if the channel requires service.

5. As to claim 2, Parvin et al teach at least one or the plurality of entries is a call to a sub list [fig. 15b] having a sub entries that correspond to the one or more channels, wherein one of the sub entries is services before returning to the circular list [col. 14, lines 39-49].

6. As to claim 3, Parvin et al teach evaluating [col. 12, lines 16-40] each sub entry as calls to the sub list are made from the circular list.

7. As to claim 4, Parvin et al teach evaluating [col. 12, lines 16-40] a channel associated with an entry further comprising the acts of:

determining an entry time [4 μs x 47 channels], the entry time representing how long until the channel will be evaluated again;

determining a latency [bus latency 4 μs], the latency representing how long the main memory will take to the data request;

determining a buffer time [16 samples x 20 μs/sample], the buffer time representing how long data stored in the data reservoir maintained by a direct memory access engine will last; and

determining that the channel requires service if the buffer time is less than the entry time and the latency.

8. As to claim 5, Parvin et al teach servicing each channel represented by the entries and the sub entries in a programmable response time [col. 24, lines 24-29].

9. As to claim 6, Parvin et al teach transferring data from the main memory to the data reservoir [col. 15, lines 33-42].

10. As to claims 8 and 17, Parvin et al teach a system having a main memory [RAM 212] for one or more devices [col. 15, lines 16-22], a method for servicing memory requirements of the one or more devices, the method comprising the acts of:

generating [col. 12, lines 4-8] a data reservoir by a direct memory access (DMA) engine [DMA controller 310] for the one or more devices, the data reservoir maintaining [col. 16, lines 47-54] a buffer for each of the one or more devices, wherein the DMA engine communicates with the main memory and the one or more devices with the DMA engine;

determining [col. 12, lines 16-40], by the DMA engine, whether a data request should be made to the main memory for each of the one or more devices;

for each of the one or more devices requiring service for the data request, requesting from the main memory, by the DMA engine, additional data to replenish [col. 12, lines 33-36] each buffer in the data reservoir for each of the one or more devices; and

providing [col. 16, lines 25-27] each of the one or more devices with access to each respective buffer [col. 16, lines 38-45] in the data reservoir.

11. As to claim 9, Parvin et al teach maintaining a channel buffer [col. 16, lines 47-54] for each channel associated with each of the one or more devices.

12. As to claim 10, Parvin et al teach the act of determining comprises the acts of:

evaluating [col. 12, lines 16-40; col. 23, line 51-col. 24, line 29] an entry in a list, the entry corresponding to a channel of a device, to determine if the channel is critical based on the factors of:

a buffer time [16 samples x 20 μs/sample] representing how long until the channel buffer in the data reservoir is empty;

an entry time [4 μs x 47 channels] representing how long until the channel corresponding to the entry will be evaluated again; and

a latency [bus latency 4 μs] representing a main memory response time;

making [col. 16, lines 47-54] the data request for the channel if the channel is critical; and

refraining [fig. 11, step 264] from making the data request for the channel if the channel is not critical.

13. As to claim 11, Parvin et al teach evaluating a next entry in the list, wherein the next entry corresponds [col. 17, lines 44-50] to another channel.

14. As to claim 12, Parvin et al teach placing the data request in a critical queue [request queue 374 in fig. 14].

15. As to claim 15, Parvin et al teach servicing each of the one or more devices in a programmable time period [col. 24, lines 24-29].

16. As to claim 16, Parvin et al teach replenishing each buffer in the data reservoir within a programmable time period [col. 24, lines 24-29].

17. As to claim 37, Parvin et al teach a system including one or more devices and a main memory storing data for the one or more devices, a system for servicing data requests of the one or more devices, the system comprising:

a direct memory access (DMA) engine [DMA controller 310], the DMA engine having a data reservoir [FIFOs 306] for consolidating memory buffers of the one or more devices;

a devices interface [FIFO controller 320] operably connected with the DMA engine, wherein the devices interface arbitrates [col. 2, lines 59-65; col. 16, lines 25-38] device data requests [col. 21, lines 29-33] generated by the one or more devices for data from the data reservoir; and

a memory interface [col. 15, lines 32-42] operably connected with the DMA engine, wherein the memory interface arbitrates [col. 14, lines 38-49] reservoir data requests generated by the DMA engine for data from the main memory to replenish [col. 12, lines 33-36] the data reservoir.

18. As to claim 38, Parvin et al teach the data reservoir comprising a plurality of device buffers [FIFOs 306], the plurality of device buffers storing data for the one or more devices, wherein each of the plurality of device buffers is associated with one of the one or more devices [col. 23, lines 54-64].

19. As to claim 39, Parvin et al teach each of the plurality of device buffers comprising at least one channel buffer for each channel associated with each of the one or more devices [col. 23, lines 54-64].

20. As to claim 41, Parvin et al teach the DMA engine guarantees that the device requests of the one or more devices is services within a programmable response time [col. 24, lines 24-29].

21. As to claim 42, Parvin et al teach the memory interface comprising a circular list [col. 17, lines 44-50; fig. 15a] having a plurality of entries, each entry representing one of the channels of the one or more devices, wherein the channels are evaluated [col. 12, lines 16-40] to determine if the channels are critical.

22. As to claim 43, Parvin et al teach the circular list is linked to one or more sub lists, the one or more sub lists having additional entries [col. 17, lines 44-50; fig. 15b].

23. As to claim 44, Parvin et al teach the DMA engine makes the reservoir data request for the channels that are critical [col. 16, lines 47-54].

24. Claims 27 and 36, are rejected under 35 U.S.C. 102(b) as being anticipated by Beck et al., US patent No. 5,826,101.

As to claims 27 and 36, Beck et al teach a system including a main memory [e.g., RAM 16] storing data for one or more devices [COM PORTs 50-55], a method for arbitrating [col. 8, lines 23-26] data requests from the one or more devices, the method comprising the acts of:

creating an arbitration mechanism [col. 32, lines 17-19] at a direct memory access (DMA) engine;

selecting [col. 32, lines 25-27; fig. 12a] eligible devices [such as channels 2, 4, and 5] from the one or more devices using the arbitration mechanism; and

allowing the eligible devices to make [col. 32, lines 25-27; fig. 12a] data requests to the DMA engine for one channel of each of the eligible devices.

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 28-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beck et al., US patent No. 5,826,101 as applied to claim 27 above, and further view of Witkowski et al., US patent No. 6,098,110.

As to claim 28, Witkowski et al teach an arbitration mechanism including a counter [col. 17, lines 36-53; col. 27, line 61-col. 28, line 22] is used to select eligible devices from one or more devices [ports 104, 110 and PCB 406] in a round-robin/rotating priority scheme.

Therefore, it would have been obvious to one or ordinary skill in the art at the invention was made to include the counter of Witkowski et al would increase flexibility in arbitrating data requests in a round-robin/rotating priority scheme of Beck et al's arbitration mechanism.

27. As to claim 29, Witkowski et al teach incrementing the counter after all the eligible devices have had an opportunity to make data requests [col. 25, lines 23-45].

28. As to claim 30, Witkowski et al teach performing a logic operation using device identifiers and the arbitration mechanism for each of the one or more devices, wherein

each of the one or more devices is an eligible device when the logic operation is true [fig. 5B; col. 25, lines 30-45].

29. As to claim 31, Witkowski et al teach allowing all of the devices to make data requests within a programmable time period [col. 17, lines 11-27; col. 24, lines 7-10].

30. As to claim 32, Witkowski et al teach the programmable time period is defined by the arbitration mechanism [col. 17, lines 11-27; col. 24, lines 7-10].

31. As to claim 33, Beck et al teach accessing data to a data reservoir [col. 29, lines 10-15] of the DMA engine for data according to the data requests.

32. As to claim 34, Beck et al teach sending data to a data reservoir [col. 29, lines 10-15] of the DMA engine for data in accordance with the data requests.

33. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Beck et al., US patent No. 5,826,101 as applied to claim 27 above, and further view of Parvin et al., US patent No. 6,167,465.

As to claim 35, Parvin et al teach maintaining [col. 16, lines 47-54] a data reservoir [FIFOs 306] by accessing a main memory according as determined by a memory interface.

Therefore, it would have been obvious to one of ordinary skill in the art to combine the teachings of Beck et al and Parvin et al because they both teach a DMA having a data reservoir for data access with a main memory and the Parvin et al's teaching of maintaining a data reservoir by accessing a main memory according as determined by a memory interface would increase serviceability for real-time applications of Beck et al [Beck et al: col. 2, lines 38-43].

34. Claims 14 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parvin et al., US patent No. 6,167,465 as applied to claim 8 above, and further view of Witkowski et al., US patent No. 6,098,110.

As to claims 14 and 40, Witkowski et al teach an arbitration mechanism including a counter [col. 17, lines 36-53; col. 27, line 61-col. 28, line 22] is maintained and used to select eligible devices from one or more devices [ports 104, 110 and PCB 406] and incrementing the counter after all the eligible devices have had an opportunity to make data requests [col. 25, lines 23-45]. Therefore, it would have been obvious to one of ordinary skill in the art to combine the teachings of Witkowski et al and Parvin et al because they both teach arbitrating [Parvin et al: col. 2, lines 59-65; col. 16, lines 25-38] data requests from one or more devices and the Witkowski et al's teaching of arbitration mechanism including a counter is maintained and used to select eligible devices from one or more devices and incrementing the counter after all the eligible devices have had an opportunity to make data requests would increase flexibility in dynamically establishing and maintaining DMA channels of Parvin et al.

Allowable Subject Matter

35. Claims 18-26 are allowed.

The following is an examiner's statement of reasons for allowance: The prior art of record does not teach or suggest in claims 18-26 individually or combination of placing the data request in a non-critical queue if the associated channel is not critical by the evaluation.

36. Claim 13 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ilwoo Park whose telephone number is (703) 308-7811. The examiner can normally be reached on Monday through Friday from 9:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on (703) 308-3301. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA, 4th Floor (Receptionist).

Ilwoo Park

Ilwoo Park

September 22, 20033